MIPS® Training

Additional Changes

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TLB Instructions

- TLB Instructions (New in release 3)
  - TLBINV – TLB Invalidate
    - On execution of the TLBINV instruction, the set of TLB entries with matching ASID are marked invalid, excluding those TLB entries which have their G bit set to 1.
    - The *EntryHI$_{ASID}$ field has to be set to the appropriate ASID value before executing the TLBINV instruction.*
    - Behavior of the TLBINV instruction applies to all applicable TLB entries and is unaffected by the setting of the *Wired register.*
      - All matching entries in the JTLB are also invalidated.
  - TLBINVF – TLB Invalidate flush
    - On execution of the TLBINVF instruction, all entries within range of *Index are invalidated.*
    - Behavior of the TLBINVF instruction applies to all applicable TLB entries and is unaffected by the setting of the *Wired register.*

There are 2 new instructions in the MIPS32 R3 of the architecture.

+ The TLB Invalidate instruction will invalidate all VTLB, FTLB and JTLB entries that match the ASID that is in the Entry Hi register.

+ The TLB Invalidate Flush will flush the entire VTLB or FTLB, and JTLB that contains the index in the CP0 Index register.

CP0 Register changes

- ErrCtl Register (CP0 Register 26, Select 0)
  - Bit 22 of the ErrCtl register is now defined as “L1 Data Cache (and Data Scratch Pad) ECC Capable” bit. It is a readonly bit.
  - ErrCtl register bit 31, PE (Parity Enable), enables ECC protection in ECC-capable implementations.
- DTag Hi Register (CP0 Register 29, Select 2)
  - The interAptiv Core implements a DTagHi register, which enables software to write ECC into the Tag RAM via an Index Store Tag to the D-cache instruction or an Index Store Data to either the SPRAM or D-cache.

CP0 Register changes

- EntryHi Register (CP0 Register 10, Select 0)
  - The EntryHiEHINV field has been added to support explicit invalidation of TLB entries via the TLBWI instruction.
  - When EntryHiEHINV = 1, the TLBWI instruction acts as a TLB invalidate operation, setting the hardware valid bit associated with a TLB entry to the invalid state. When EntryHiEHINV = 1, only the Index register is required to be valid.

CP0 Register changes

- CacheErr Register (CP0 Register 27, Select 0)
  - ER:EC has a new code for a corrected ECC error of 11
- Config0 Register (CP0 Register 16, Select 0)
  - K23, KU, and MT in the Config register are no longer present.
- Config3 (CP0 Register 16, Select 3)
  - new SC bit (25) to indicate Segmentation control is implemented.
- Config4 (CP0 Register 16, Select 4)
  - TLBINV, TLBINVF instructions supported. IE bit 30:29 setting to 10.

ER-EC field in the Cache error register has a new code of 11 to indicate a corrected ECC error

The Config0 K23 and KU fields are not longer present because there is no KSEG 2 or 3 or KUSEG

The MT field is no longer present because the interAptive CORE can only have TLB memory translation

Feature Changes

- Only 8 way L2 cache support
- Branch History and Return Pointer Stack always present.
- TLB is not a option it will always be present and therefore the cores cannot not have a FMT type of MMU.
- Cannot Share TLB between VPEs

Here are features that have changed. None of them will effect coding.